TESTING CARD

This application claims the benefit of Taiwan application Serial No. 92100644, filed Jan. 13, 2003.

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The invention relates in general to a testing card, and more particularly to an integrated testing card.

Description of the Related Art

[0002] With the rapid advance in science and technology, a large variety of electronic products have been developed in recent years. Take the personal digital assistant (PDA) for example. Within only a few years' time, its screen has been upgraded from mono-color screen to full-color screen; its size is further reduced while its functions are further augmented. Nowadays, the PDA has almost become an indispensable handy device to business people.

[0003] To satisfy its user's strong need for function augmentation, a PDA is normally equipped with at least one card interface for the augmentation of functions. For example, a personal computer memory card international association card (PCMCIA card) or a compact flash card (CF card) can be used as a memory card or an input/output card (I/O card) to enhance the

function of a PDA. The abovementioned I/O card can be a modem card for instance.

[0004] From the manufacturer's point of view, a product must pass a series of inspections and tests to assure its quality before the product is allowed to leave the factory. The function test of the card interface is a very important test to be performed. Whatever card interface an electronic product may use, no matter it is a PCMCIA card, a CF card or other card interfaces, the card interface used must have memory support and I/O support functions to satisfy the user's diverse needs of augmentation. The most common way of testing is conducted by using ordinary memory card and I/O card respectively to test the memory function and the I/O function of a card interface. During the process of testing, the memory card will be inserted into the card slot for memory access test and will be removed from the card slot after memory test is finished; then the I/O card will be inserted into the card slot to test the input/output signal. Despite that the inspector has already tested the memory function and I/O function of a card interface using a memory card and an I/O card respectively, there are always some signals to be tested being left out. For example, if mode selection signal IOIS16, wait signals WAIT and interrupt signal INT are left out, the reliability of quality assurance will decrease. Besides, to test the interface memory and the interface I/O function of testing card, the inspector needs to use a memory card and an I/O card respectively, not only a longer duration of test is needed but also a smooth flow of testing process will be interrupted. For

example, excluding the loading/unloading time, it still takes 7 seconds to test the ATA-Type memory card and 25 seconds to test the I/O card.

SUMMARY OF THE INVENTION

[0005] It is therefore an object of the invention to provide a testing card which integrates all interface signals to be tested such as memory signals and input/output signals into a single card to shorten the testing time and simplify the testing process as well.

[0006] According to the object of the present invention, a testing card is provided and disclosed below.

[0007] The testing card is used to be coupled to the card interface installed in an electronic device to test the function of the card interface. The testing card comprises a converting circuit, a latch circuit, a data processor, a signal generator, an oscillation combination circuit, and a reset circuit. The converting circuit is used to receive the attribute control signal, the common memory signal and the input/output signal fed in from the card interface, convert these signals and output them to the data processor afterwards. The latch circuit is used to receive the data signal fed in from the card interface, latch the data signal and output it to the data processor afterwards. Having received the signal sent from the converting circuit and the latch circuit, the data processor will be able to proceed with testing accordingly. The signal generator can output the mode selection signal and the interrupt signal

to the card interface to test the functions of mode selection and interrupt signals. Furthermore, the signal generator outputs the enable signal to the oscillation combination circuit according to the control signal fed in from the card interface, so that the oscillation combination circuit can generate a wait signal according to the enable signal and feed the wait signal to the card interface for testing purpose. The reset circuit is used to reset the above latch circuit, data processor, signal generator and oscillation combination circuit to start the testing process again.

[0008] The testing process performed by the testing card according to the present invention includes the following procedures:

[0009] Firstly, identify the testing card. Perform 16 bits I/O addressing mode test if the identification is successful; otherwise display an error message if the identification fails. Next, proceed with 16 bits attribute addressing mode test if the 16 bits I/O addressing mode test is successful; otherwise, display an error message if the 16 bits I/O addressing mode test fails. Perform memory addressing mode test if the 16 bits I/O attribute addressing mode test is successful; otherwise, display an error message if the 16 bits I/O memory addressing mode test fails. Set the testing mode to 8 bits and perform 8 bits I/O addressing mode test if the memory addressing mode is successful; otherwise, display an error message if the memory addressing mode test fails. Perform wait signal test if the 8 bits I/O addressing mode test is successful; otherwise, display an error message if the 8 bits I/O addressing mode test fails. During the wait signal test, first of

all, the wait signal is enabled and counting process is executed; after that, the wait signal is disabled, the counting process is executed. Meanwhile, whether the wait signal complies with the standard or not will be determined according to the difference between the counting result obtained when the wait signal is enabled and the counting result obtained when the wait signal is disabled. Conclude the testing process if the wait signal complies with the standard; otherwise, display an error message if the wait signal fails to meet the standard.

[0010] Other objects, features, and advantages of the invention will become apparent from the following detailed description of the preferred but non-limiting embodiments. The following description is made with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. 1 is a block diagram for a testing card according to a preferred embodiment of the invention; and

[0012] FIG. 2A ~ 2C are flowcharts showing testing method performed by the testing card in FIG. 1.

DETAILED DESCRIPTION OF THE INVENTION

[0013] Please refer to FIG. 1, a block diagram for a testing card according to a preferred embodiment of the present invention. The testing card is used

to be coupled to card interface 110 installed in an electronic device to test the functions of card interface 110 wherein the electronic device can be a personal digital assistant for instance. The testing card includes converting circuit 130, latch circuit 150, data processor 140, signal generator 170, oscillation combination circuit 180 and reset circuit 160, wherein data processor 140 can be embodied using a flash memory and can measure interface signals using the firmware burnt onto data processor 140. For the testing card to test both memory function and I/O function, converting circuit 130 must be able to process attribute control signal ATTR, common memory signal COMM and input/output signal IO coming from card interface 110. Conventionally, only attribute control signal ATTR and common memory signal COMM can be tested during memory card testing, while only attribute control signal ATTR and input/output signal IO can be tested during input/output signal testing. Compared with the conventional testing method which cannot test attribute control signal ATTR, common memory signal COMM and input/output signal at the same time, converting circuit 130 according to the invention can test the three signals at the same time, integrating the memory function testing and the input/output signal function testing together.

[0014] Latch circuit 150 can latch data signal DATA coming from card interface 110. The memory function testing and the input/output signal function testing can be performed when the data signal DATA is fed into data processor 140 in conjunction with address signal AD. As the testing process

proceeds, data processor 140 will sequentially test 16 bits input/output signal IO, 16 bits attribute control signal ATTR, common memory signal COMM and 8 bits input/output signal IO. The testing process will be further elaborated below.

[0015] Signal generator 170 generates mode selection signal IOMD and interrupt signal INT, the two signals that cannot be obtained in conventional testing process by inserting either a memory card or an I/O card. The invention uses signal generator 170 to generate both mode selection signal IOMD and interrupt signal INT, then feed the two signals into card interface 110 in conjunction with the firmware of the data processor so that the operation of selection signal IOMD and interrupt signal INT can be tested and determined.

[0016] Moreover, signal generator 170 can generate enable signal EN according to control signal CT fed in from card interface 110, and feed the enable signal EN to oscillation combination circuit 180 to generate wait signal WAIT wherein enable signal EN can be a negative trigger signal. When enable signal EN is at high levels, wait signal WAIT will be at high levels as well and will be disabled accordingly. At the same time, the CPU operation capacity of the electronic device will not be interfered with. Data processor 140 can set the CPU to count a pre-determined number, 1000 for instance, and record the time needed to finish the counting, say, T1 for instance. When enable signal EN drops from a high level to a low level, oscillation combination circuit 180 will generate a square-wave signal with high level

signals alternating with low level signals. Wait signal WAIT will be enabled when it is at low levels, so CPU will stop when wait signal WAIT is at low levels. The operation speed of CPU will slow down when the square-wave signal which enables wait signal WAIT intermittently is fed into the CPU. Meanwhile, data processor 140 can again set the CPU to count a pre-determined number, say, 1000 for instance, and record the time needed to finish the counting, say, T2 for instance. Subtract T2 from T1 and examine the difference, whether the operation of wait signal WAIT complies with the standard or not can thus be determined. By doing so, whether wait signal WAIT function normally or not can also be determined.

[0017] The function of reset circuit 160 is to reset these latch circuit 150, data processor 140, signal generator 170 and oscillation combination circuit 180, so that the testing card can re-start testing for next card interface 110.

[0018] Please refer to FIG. 2A ~ 2C, flowcharts showing testing method performed by the testing card in FIG. 1. Firstly, identify the testing card (step 210). If the identification is successful, perform 16 bits I/O addressing mode test for the test of 16 bits input/output signal IO (step 215, 220); otherwise display an error message if the identification fails. Meanwhile, mode selection signal IOMD can be set at a low level to test the erase signal, the write signal, the read signal and the compare signal. The 16 bits I/O addressing mode test covers address signals of lower levels, data signals, PIOW signals and PIOR signals of input/output signal IO.

[0019] If the 16 bits I/O addressing mode test is successful (step 225), proceed with 16 bits attribute addressing mode for the test of 16 bits attribute control signal ATTR (step 230); otherwise, display an error message if the 16 bits I/O addressing mode test fails. The 16 bits attribute addressing mode test, which tests the erase signal, the write signal, the read signal and the compare signal, covers the PWE signal and POE signal of attribute control signal ATTR.

[0020] If 16 bits I/O attribute addressing mode test is successful (step 235), perform memory addressing mode test (step 240); otherwise, display an error message if 16 bits I/O memory addressing mode test fails. Memory addressing mode test, which covers higher level address and data signals, can test the common memory signal. If memory addressing mode test is successful (step 245), set mode selection mode IOMD at high levels and set testing mode to be at 8 bits (step 250) to proceed with 8 bits I/O addressing mode test (step 255); otherwise, display an error message if memory addressing mode test fails. The 8 bits addressing mode test, which tests the erase signal, the write signal, the read signal and the compare signal, covers various testing results obtained when mode selection signal IOMD is set at high levels.

[0021] If 8 bits I/O addressing mode test is successful (step 260), perform wait signal test; otherwise, display an error message if the 8 bits I/O addressing mode test fails. Firstly, use the square wave as wait signal WAIT which can be enabled, and set the CPU to count a pre-determined number,

1000 for instance, and record the time needed to finish the counting, say, T2 for instance, (step 265). Next, continue to set wait signal WAIT at high levels; wait signal WAIT is actually disabled. Again, set the CPU to count a pre-determined number, 1000 for instance, and record the time needed to finish the counting, say, T1 for instance, (step 270). Whether wait signal WAIT complies with the standard or not can thus be determined according to the difference (T2-T1) which is obtained when wait signal WAIT is enabled and disabled respectively (step 275). If the standard has been met, conclude the testing process (step 280); otherwise, display an error message.

[0022] The testing card disclosed in the above preferred embodiment according to the invention can be applied to various operating systems such as WinCE, Palm or Linux. For the abovementioned testing structure and process to be applied to various operating systems, only slight firmware modifications for respective data processor are needed. For those who are familiar with this technology, such conversion is not a problem at all.

[0023] To summarize the above disclosures, the testing card according to the preferred embodiment of the invention has at least the following advantages:

[0024] 1. that the memory signal and the input/output signal being tested at the same time saves a large amount of testing time and testing process;

[0025] 2. that only one single testing card is needed to complete memory

test and input/output signal test makes it much cheaper compared with the conventional testing method which requires a memory card and an I/O card respectively;

[0026] 3. that a wider range of hardware interface signals including mode selection signal, interrupt signal and wait signal etc. can be tested; and

[0027] 4. that the use of flash memory as an embodiment of data processor provides upgrading and storage functions for the testing program.

[0028] While the invention has been described by way of example and in terms of preferred embodiments, it is to be understood that the invention is not limited thereto. On the contrary, it is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.